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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,973	04/05/2001	Norio Hirashita	OKI.227	3710

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/825,973	Applicant(s) HIRASHITA ET AL.	
	Examiner Julio J. Maldonado	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,24,26,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,7,8,11,12,15,16,24,26,28,30,32 and 34* is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,13,14,31 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 9, 13, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (U.S. 6,344,675 B1) in view of Gallagher et al. (U.S. 4,968,644).

Imai (Figs.12-13D) teach a low resistance SOI-FET device including an insulating layer (2); a semiconductor layer (3) formed on the insulating layer (2), wherein the semiconductor layer (3) includes the channel region therein; a pair of impurity layers (9, 10) formed in regions which are respectively in contact with the channel region in the source region and the drain region; and a pair of metallic silicide layers (16) respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers (16) are respectively in contact with the pair of impurity layers (9, 10), wherein bottom surfaces of the pair of metallic silicide layers (16) extend to bottom surfaces of the semiconductor layer (3), wherein the thickness of the metallic silicide layers (16) is equal to or more than 80% of form an upper surface of the metallic silicide layers (16) to the bottom surface of the semiconductor layer; wherein the metallic silicide layers (16) are composed of refractory metal and silicon, and wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, wherein the metallic silicide layer

comprises cobalt silicide (column 22, line 66 – column 25 line 21 and column 43, line 6 – column 48, line 63).

Furthermore, Imai in another embodiment of the invention teaches wherein the source and drain regions extend between the cobalt silicide layers formed in said source and drain regions and the bottom surface of the semiconductor region (see, Fig.10).

Imai fails to teach wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than $1x10^{-7}\Omega\text{-cm}^{-2}$.

However, Gallagher et al. (Figs.1-7) teach a low resistance FET device including a pair of silicide layers (not shown) respectively in contact with a pair of impurity layer (80, 90) of the FET device, wherein said silicide layers include cobalt silicide, and wherein adding silicide layers to a contact region have the advantage of thermally stable contact resistivities, which are lower than $1x10^{-7}\Omega\text{-cm}^{-2}$ (Gallagher et al., column 10, lines 15 – 28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imai and Gallagher et al. to enable using the silicide layers of Gallagher et al. in the FET structure of Imai for the further advantage of reduced contact resistivities (Gallagher et al., column 10, liens 15 – 28).

Still the combined teachings Imai and Gallagher et al. fail to teach wherein the semiconductor layer has a thickness of 20 nm. One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and

optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

3. Claims 2, 6, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai ('675 B1) in view of in view of Gallagher et al. ('644) as applied to claims 1, 5, 9, 13, 31 and 33 above, and further in view of the Applicants Admitted Prior Art.

The combined teachings of Imai and Gallagher et al. substantially teaches all aspects of the invention but fails to show wherein said FET device includes a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof. However, the prior art teaches FET devices include a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof (Instant pages 1 – 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imai and

Gallagher et al. with the prior art to enable including the structure resulting in the depletion layer of the prior art in the device of Imai and Gallagher et al.

Allowable Subject Matter

4. Claims 3, 4, 7, 8, 11, 12, 15, 16, 24, 26, 28, 30, 32 and 34 are allowed.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 2, 5, 6, 9, 10, 13, 14, 31 and 33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
April 13, 2006

GEORGE R. FOURSON
PRIMARY EXAMINER